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B022314(022)

B. Tech. (Third Semester) Examination, Nov.-Dec. 2020

(Computer Science and Engg. Branch)

DIGITAL ELECTRONICS and LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note *: Attempt all questions. Each question carries equal makrs. Part (a) is compulsory and answer any* ***two*** *parts from (b), (c) and (d).*

1. (a) Fill in the blanks : 4

(i) (84-2-1) code for decimal digit 3 is .....

(ii) 2's complement of 101100 is .....

(iii) Binary of gray code 00110110 is .....

(iv) Excess 3 code of decimal number 9 is .....

(b) Solve the following using K-map : 8

(i) $F1(A, B, C, D) = \Sigma m(1, 5, 6, 12, 13, 14) + \Sigma d(24)$

(ii) $F2(A, B, C, D) = \Pi m(0, 1, 2, 4, 6, 8, 9, 11, 12)$

(c) Simplify the following using Tabulation method : 8

$F(A, B, C, D) = \Sigma m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$

(d) The message below coded in the 7-bit hamming code is transmitted through channel. Decode the message assuming that single error occurred in each code word.

(i) 1001001

(ii) 0111001

(iii) 1110110

(iv) 0011011

Find the correct code in each case. 8

2. (a) Compare RTL, DTL, TTL and ECL on the basis of : 4

(i) Component used

(ii) Fan out

(iii) Propagation delay and

(iv) Application

(b) With the help of neat diagram, explain the working of :

(i) CMOS inverter and

(ii) CMOS NOR gate 8

(c) Explain the working of TTL circuit with Totem pole output configuration. 8

(d) Implement the fgollowing Boolean function using : 8

(i) PLA

(ii) PLA

$F1(A, B, C) = \Sigma m(3, 4, 5, 6, 7)$

$F2(A, B, C) = \Sigma m(2, 5, 6, 7)$

3. (a) Fill in the blanks : 4

(i) ..... consists of logic gates where output at any instant is determined by present combination of input as well as previous state of output.

(ii) ..... is an example of combinational circuit.

(iii) Logical expression of carry out in half adder is .....

(iv) Minimum number of NAND gates required for designing Half Adder is .....

(b) Design 4-bit look ahead carry adder with suitable diagram. 8

(c) Design full adder using 4 : 1 MUX. 8

(d) Design and implement comparator. 8

4. (a) Convert SR flip-flop to T flip-flop. 4

(b) What is race around condition for J-K flip-flop? How it can be avoided in master slave flip-flop? 8

(c) Design and implement 4 bit synchronous up counter. 8

(d) Design Serial in Serial Out (SISO) and parallel in Serial Out (PISO) shift register using D flip-flop. 8

5. (a) Discuss the various operators used in VHDL. 4

(b) Write short notes on Mealy and Moore machine. 8

(c) Write a program in VHDL using data flow modelling for half adder. 8

(d) Write a program in VHDL using behavioural modelling for AND gate. 8